Simulating Electrostatic Discharge

Dejan Maksimović, Guido Notermans

Abstract - In this paper we justify the necessity of the electrostatic discharge simulation. We give an overview of the ESD stress standards and the ESD protection devices. We further describe the modelling of the ESD devices and give a case study which shows the importance of timely ESD simulation for the design success.

Keywords – ESD, simulation, modelling, HBM, MM, CDM, HMM.

I. Introduction

Electrostatic discharge (ESD) occurs between two bodies at different electrostatic potentials. The charging of these bodies can occur either by triboelectricity or by induction. ESD is characterized by a short duration (0.1ns to 100ns), high current (1A to 30A) pulse. Such high current can damage the semiconductor device. Failures can be thermally induced due to the high power dissipated during the ESD event: silicon melting can be observed as well as metal or polysilicon resistance blow-up if the metal/poly line is not designed wide enough. Gate oxide breakdown can also be observed due to the large voltage drop bult-up by the ESD current.

ESD can occur any time in the life of the product: during manufacturing, assembly, testing, shipment and in the final application and it is a key issue for the reliability of the integrated circuits (ICs).

Two approaches are used together to fight against the ESD. The first one is to prevent the ESD events. Special dissipative materials are used in clean rooms and labs, ionizers, proper grounding of the equipment, wearing of a wrist strap during the tests etc. The second approach is to implement efficient ESD protection on the IC. The ideal ESD protection circuit is similar to a switch: it is highly resistive during the normal operation of the IC, but it is able to detect an ESD event and to become low resistive when it occurs. In such a way the ESD device shunts the ESD current with the lowest possible voltage drop.

Dejan Maksimović and Guido Notermans are with the ST-Ericsson, Binzstrasse 44, 8045 Zurich, Switzerland, E-mail: dejan.maksimovic@stericsson.com, guido.notermans@stericsson.com .

II. Modeling the ESD Events

There are many ESD models, three of them being the most widely used: human body model (HBM), machine model (MM) and charged device model (CDM).

2A. Human Body Model (HBM)

This model corresponds to the discharge of a charged human being into the IC. The capacitance of the average human body (to ground) is 100pF. The average skin resistance is 1.5kOhm. The body capacitance is charged to a certain voltage level and discharged throuth the skin resistance and the device under test (DUT) to the ground. The electronic circuit representing this event is shown in Figure. 2.1.

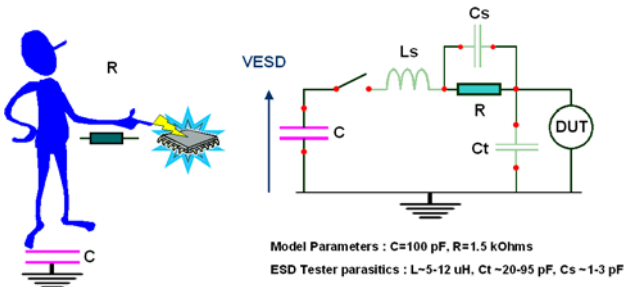

Fig. 2.1. Human Body Model (HBM).

This ESD model is defined by the JEDEC standard JESD22-A114F [1].

2B. Machine Model (MM)

This model emulates the discharge that can occur in automatic assembly lines between a machine and the IC. The charged machine has a higher capacitance of 200pF, while the contact resistance is very low, almost zero, often considered as a few ohms. Due to the low resistance, this model is strongly dependent on the parasitic inductance which has to be fixed and is in the order of 0.5uH. The electronic circuit representing this kind of ESD event is shown in Figure. 2.2.

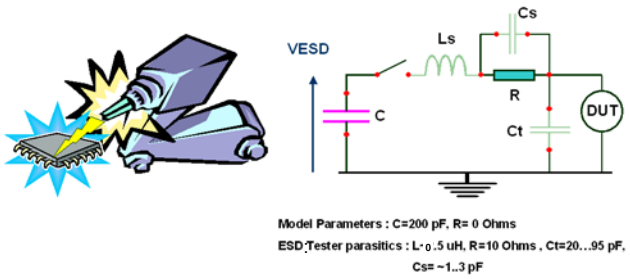

Fig. 2.2. Machine Model (MM).

This ESD model is defined by the IEA/JEDEC standard IEA/JESD22-A115-A [2].

2C. Charged Device Model (CDM)

This model emulates the discharge of a charged IC to the ground which occurs when one pin of the IC touches a grounded surface. The whole IC is charged and the discharge is determined by many device parameters such as the package type and the die size. The CDM event is very short (rise time is less than 0.5ns) high current pulse in order of tens of amperes. It mostly causes the gate oxide failures due to the overvoltage caused by such a high current. A typical CDM current waveform is shown in Figure 2.3.

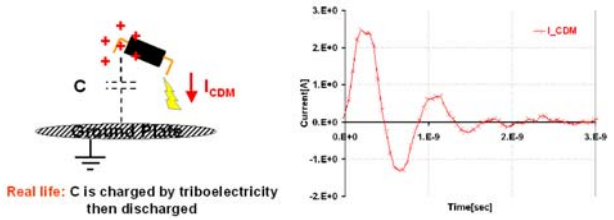

Fig. 2.3. Charged Device Model (CDM).

During the CDM test the device is placed in a "dead bug" position on a charging plane connected to a high voltage source. Above the device there is a ground plane. The discharge occurs when the pogo pin connected to the ground plane touches one pin of the IC. This ESD model is defined by the JEDEC standard JESD22-C101C [3].

While the HBM and MM events occur between two pins of the IC and the circuit can be designed in such a way that the ESD current path is predictable, during the CDM stress the current comes from the silicon substrate and distributes in an unpredictable way through the metal lines and devices towards the stressed pin.

2D. System Level ESD Stress (Gun Test)

This model corresponds to the "real-world" discharge that happens when the final user handles the product that contains the IC. The stress levels are much higher and the test is performed using the ESD gun. The discharge is applied to every possible exposed surface of the product, such as metal connectors, displays, case, etc. The ESD current flows from the stressed point to the system ground (and another way around), which is similar to the CDM discharge. The current waveform is shown in Fig. 2.4. It consists of a very short CDM-like first pulse of very high amplitude and a HBM-like second pulse of the amplitude higher than that of the HBM pulse for the same stress level. The gun pulse parameters for different stress levels are given in Table 2.1.

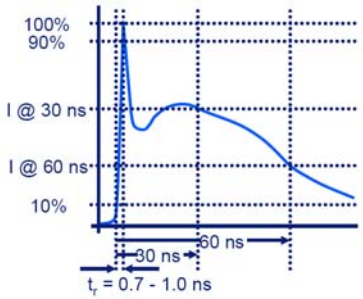

Fig. 2.4. Gun test current waveform.

TABLE 2.1
GUN TEST CURRENT WAVEFORM PARAMETERS FOR DIFFERENT STRESS LEVELS

Level	Indicated voltage [kV]	First peak current of discharge ±10% [A]	Rise time tr contact discharge [ns]	Current (±30%) at 30 ns [A]	Current (±30%) at 60 ns [A]
1	2	7.5	0.7-1.0	4	2
2	4	15	0.7-1.0	8	4
3	6	22.5	0.7-1.0	12	6
4	8	30	0.7-1.0	16	8

TABLE 2.2
HBM PEAK CURRENT VERSUS THE FIRST PEAK AMPLITUDE IN THE GUN TEST

Applied voltage [kV]	HBM peak current [A]	Gun test first peak current [A]
2	1.33	7.5
4	2.67	15.0
6	4.00	22.5
8	5.33	30.0
10	6.67	37.5

This ESD model is defined by the IEC standard 61000-4-2 [4]. Table 2.2 compares the maximum peak current during the HBM and gun test for the same voltage levels [5].

2E. Transmission Line Pulse (TLP) Measurement

The ESD tests described so far are pass/fail measurements. They do not give any information on the behaviour of the IC during the ESD event. To obtain I(V) characteristics of the ESD protection circuits and devices a special tool called TLP is used [6].

During the TLP measurement, the DUT is subjected to a trapezoidal positive current pulse. Once the transients in

the device are over, the current through and the voltage over the DUT are measured. This produces one I/V data point. To check if the device is still not damaged, the DC leakage through the DUT is measured after each I/V data point extraction. If no degradation is observed, the amplitude of the current pulse is increased and the next data point is measured. In this way the I(V) curve of the device can be constructed starting from the low ESD currents and finishing after the device is damaged.

The TLP can vary the rise time and/or the width of the current pulse. The most commonly used parameter values are Tr=10ns, Tw=100ns. The I/V data point is usually taken at 90% of the Tw, i.e. after 90ns.

The current and voltage waveforms during the TLP measurement look like those shown in Fig. 2.5. The waveforms in Fig. 2.5 were obtained by the electrical simulation though.

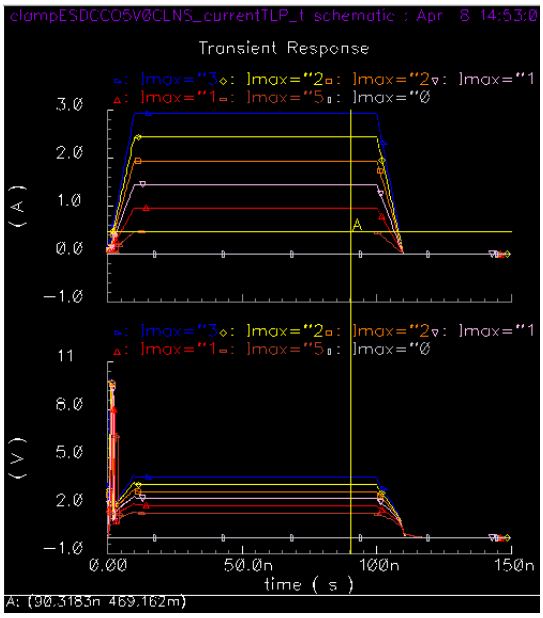

Fig. 2.5. The TLP waveforms obtained by the simulation. The measurement point at 90% of pulse width is shown.

A typical measured TLP curve of an ESD device is shown in Fig. 2.6.

2F. Definition of ESD Parameters

The most important ESD parameters are shown on the TLP curve in Fig. 2.6. They are as follows:

Vt1: Trigger voltage. This voltage must not be higher than the (gate oxide or PN junction) breakdown voltage of the circuitry connected in parallel to the ESD device. In case the device does not exhibit the snap-back (like in the case of the diode), this parameter is sometimes called Von.

Vh: Hold voltage. Minimum voltage on the ESD device is important since if it is below the supply voltage of the IC, the ESD event can cause the latch-up (large leakage from the supply to the ground that can be stopped only if the supply is turned off).

It2 – Failure current. This is the maximum ESD current that the ESD device can conduct without being damaged.

Vt2 – Voltage at failure level. This parameter is important only if Vt2>Vt1.

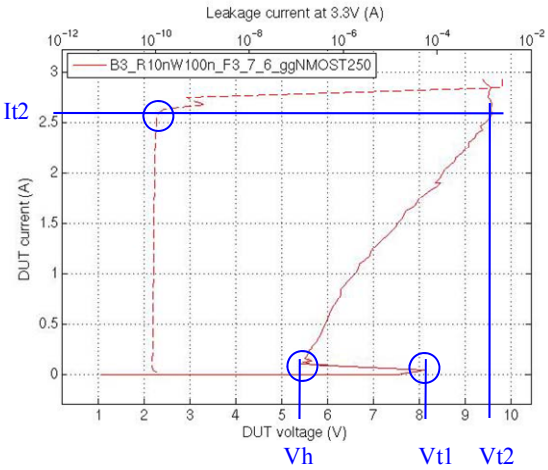

Fig. 2.6. Typical TLP characteristic of a ggNMOST with the ESD parameters marked.

2G. Correlation between different ESD stresses and TLP

A 100ns current pulse delivers a thermal stress equivalent to the HBM stress. A good correlation has been reported between the TLP It2 value and the HBM fail level: the device which fails at 2kV HBM level will also fail at 1.33A TLP current if 100ns wide pulse is applied. Hence, there is a correlation factor of approximately 2kV/1.33A=1.5kV$_{HBM}$/A$_{TLP}$ between the It2 in TLP curve and the HBM fail level.

The HBM and MM produce similar IC failures and there is a relation between them: typically 2kV HBM level corresponds to 100V MM level (ratio 20 times). Consequently, the correlation factor between the MM fail level and the It2 is approximately 75V$_{MM}$/A$_{TLP}$.

The relation between IEC and TLP stress is: 1A TLP corresponds to 600V IEC gun test [7]. This results in 13.3A TLP current for 8kV IEC.

III. ESD Protection Devices

Early in the design process, the ESD protection concept is being discussed and planned. There are two main approaches: local ESD protection and rail-based ESD protection. If the ESD protection is implemented locally, then each pin of the IC has its own ESD protection element

(also known as "local ESD clamp"). In rail-based concept, the protection elements are connected only between the power and ground rails (rail clamps). The ESD current is diverted from each input/output (I/O) pin using the ESD diodes connected between the I/O pin and the power rail and between the I/O pin and the ground rail.

There are many different types of ESD protection devices. Some of them will be shortly described here.

3A. Diodes

Diodes are used in forward bias to conduct large ESD currents. The forward biased diode can conduct between 5mA and 30mA per micrometer of the junction perimeter (typically 10ma/um). In the inverse (Zener) breakdown the diode can however conduct very small ammount of ESD current.

The problem that often arises when one wants to simulate the ESD is that the diodes are not properly modelled in forward bias. This because the diodes are very rarely used in functional part of the IC – they are only the parasitic junctions and are supposed to always remain inverse biased. ESD diodes are however an exception to this rule.

3B. Snap-back devices

The most popular snap-back devices are ggNMOST and thyristor (also known as silicon-controlled rectifier – SCR). They have the I(V) characteristic similar to that in Fig. 2.6. Due to the negative resistance region in the curve, they cannot be simulated. SCRs have much deeper snap-back (lower Vh) than the ggNMOSTs.

It is important to say that each NMOST (or PMOST) can be driven into the bipolar mode and experience the snap-back. For this to happen, the voltage between their drain and source must reach the inverse breakdown of the drain/bulk junction. Of course, this is an unwanted event and it is sometimes possible to simulate the surrounding circuitry to discover if the critical voltage is reached on the MOS transistor.

3C. BigFETs

If a large NMOS transistor is conducting in parallel to the protected circuitry during the ESD pulse, it can take over all the ESD current and such protect the rest of the circuit. This ESD device is known as bigFET (or RC triggered FET) and is used as a rail clamp in most of the modern CMOS technologies. BigFET triggers at around 1V (slightly higher than a diode) and has a special RC circuit which is responsible to switch it off after the ESD pulse is over. Since all the circuitry in this clamp is working in normal MOS operation mode, the device can be simulated.

IV. ESD SIMULATION

To be able to simulate the ESD event two models are necessary:

- the model of the ESD current pulse

- the model of all the ESD (and other) components in the circuitry connected to the stressed IC pin.

Both models can be easily developed for the analog simulator. The stimulus generator is made using a circuit such as that in Fig. 2.1 and 2.2. The waveform is adjusted to that prescribed by the corresponding ESD test standard.

The ESD devices are usually produced on a test wafer and TLP measured to extract their electrical parameters. Then the electrical model is built using these parameters and used in ESD simulation.

A few examples of ESD simulations on the device level will be given in following paragraphs.

4A. Generating the TLP characteristic of the bigFET clamp

The TLP tester is used for on-wafer measurements. The test circuit often contains additional resistance of metal connections from the ESD device to the measurement pads. Therefore the measured TLP curve has higher resistance than the ESD device itself.

If the ESD device is of the kind that can be simulated, such as a bigFET clamp, the simulation can show us the real resistance. The Fig. 4.1 shows a simple simulation testbench with such a bigFET rail clamp.

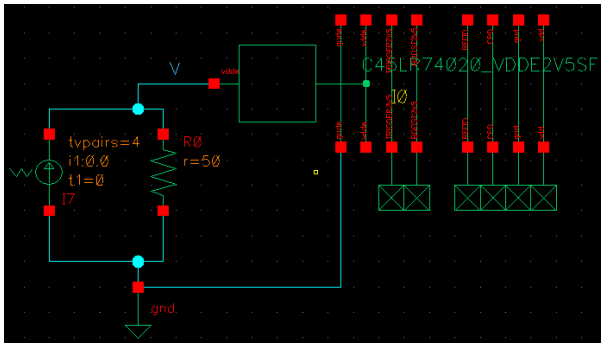

Fig. 4.1. Testbench for generating the TLP characteristic of the clamp by the simulation.

The trapezoidal current generator and the 50ohm resistor model the TLP system. The current and voltage waveforms obtained by the simulation are shown in Fig. 2.5. The parametric analysis is used to change the amplitude of the current pulse with constant step. Same as in TLP system, the I/V points are measured at 90ns simulation time.

The resulting TLP curves of a few different types of clamps are shown in Fig. 4.2. It must be stressed that the transistor models are valid only in the nominal supply range (up to 5V in this case). The simulations we did here by far exceed this range. This means the curves can be trusted only up to 5V. Nevertheless, the TLP measurements and long experience in this technology process show us that the clamp does not change the resistance until very close to the destruction level. The failure level can only be determined by the TLP measurement on the silicon. The simulation cannot give us this information. However, even the TLP can measure only up to 10A and above this point we cannot judge the behaviour of the devices which are designed for higher currents.

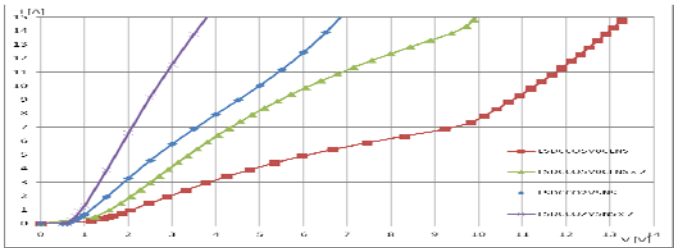

Fig. 4.2. Simulation waveforms.

To eliminate the simulation artefacts (invalid simulation results due to too high voltages), we can interpolate the clamp curves obtained by the simulation in the valid range as shown in Fig. 4.3. This enables us to estimate the voltage drop on the clamp in case of different ESD stresses and help us decide if we need to use more than one clamp in parallel to reduce the voltage.

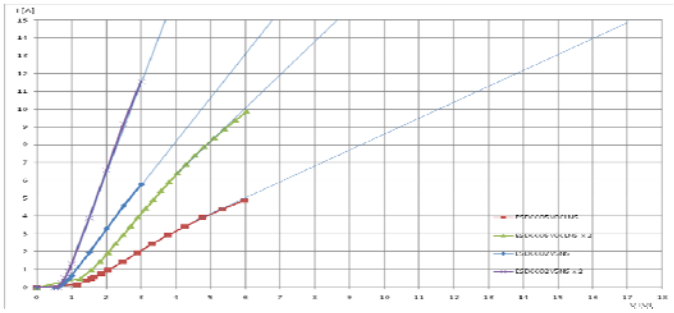

Fig. 4.3. Linear interpolation of the TLP curves generated by the simulation outside of the valid range of the circuit models.

B. Simulating a bigFET clamp under the CDM stress

The testbench schematic for the simulation of the CDM stress influence on the clamp is shown in Fig. 4.4. The sinewave current generator emulates the CDM pulse. The CDM pulse is approximately 2ns long positive pulse of certain amplitude. The negative half-period of the used sine generator is not important – the reverse diode of the clamp will conduct during it. The results of the simulation are shown in Fig. 4.5.

First of all, during the negative half-period of the current pulse, the simulation shows only 1V over the reverse diode of the clamp. This is definitely an underestimation – the diode model is obviously not valid in forward bias.

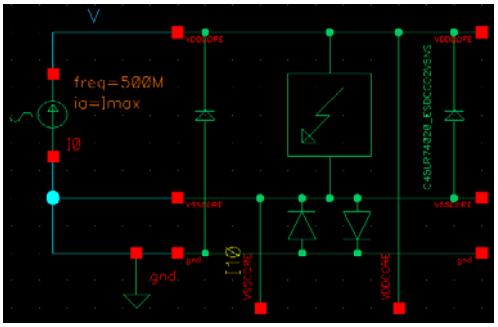

Fig. 4.4. A simple simulation testbench for the CDM stress.

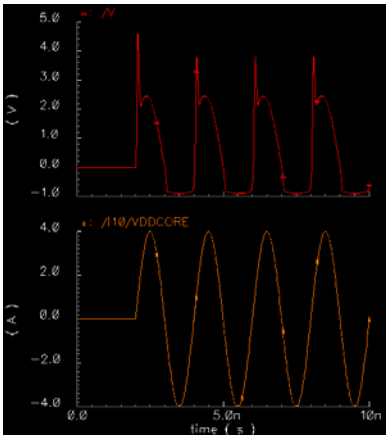

Fig. 4.5. CDM simulation waveforms.

During the positive half-period of the current pulse the voltage on the clamp shows a short, very high peak. This peak is the consequence of the bad design of the clamp. The clamp cannot trigger fast enough to conduct the CDM pulse. Some time later, the clamp triggers and this pulse falls down (clamp resistance is reduced) to 2V. This voltage is realistic to expect for this kind of the clamp when conducting a 4A current.

From this simulation we can conclude that the clamp triggering is not fast enough if 4A CDM peak current is to be expected from the IC.

V. A CASE STUDY

A simplified schematic of the output stage of the radio antenna in an IC is shown in Fig. 5.1. The power amplifier has a PMOST connected between the VDD_PA and the antenna pin Int_Ant. The bulk diode of the PMOST (Dpmost) is also shown in the schematic. The wire resistance between the PMOST drain and the Int_Ant pad is around 2ohm. The voltage at the antenna pin can vary between -2V and +2V. Therefore, the four-diode string (D11-D14 and D21-D24) is used as the ESD protection on this pin. The rest of the circuit is protected with a standard

rail-based ESD concept, which assumes the rail clamps (bigFETs) between the power (VDD_PA) and ground (VSS_PA) rail. In the shown voltage domain two such clamps are connected (C1 and C2). Each rail clamp has the reverse diode (Dr_{C1} and Dr_{C2}).

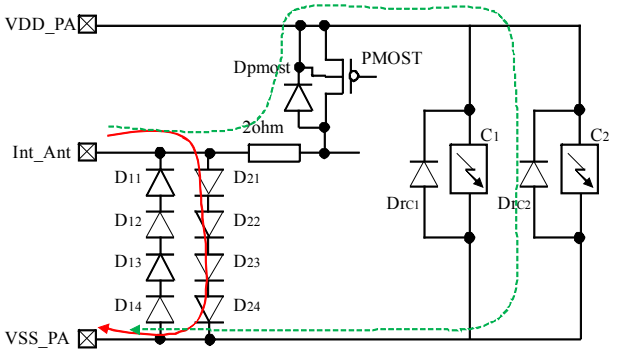

Fig. 5.1. ESD protection and functional circuitry at the antenna pin of an FM radio IC.

The Int_Ant pin is supposed to withstand 8kV system level stress (gun test) without adding any additional external ESD protection on the application board. The intended ESD current path for the current between Int_Ant and VSS_PA is through the 4-diode string (depicted with red line in Fig. 5.1). There is however the alternative path through Dpmost and clamps C1/C2, as shown by the dashed green line in Fig. 5.1. This unwanted current could damage some of these devices. To prevent this, the circuit was modeled and simulated before the production.

The 4-diode strings are designed to be able to conduct 14A of the 100ns TLP current. Their TLP characteristics measured on a separate test wafer are shown in Fig. 5.2. The TLP tester could produce maximum current of 10A, hence the diodes could not be damaged. The diode curve was estimated up to 14A by removing the connection resistance (depicted red in Fig. 5.2). The simulation model was generated with Von=4V and Ron=0.25ohm, same in both directions.

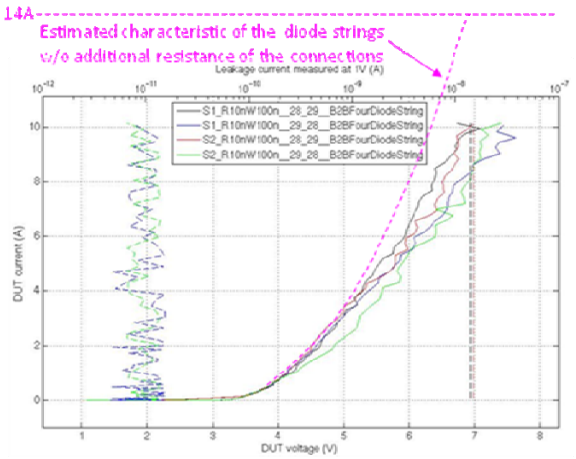

Fig. 5.2. Measured TLP characteristics of the 4-diode string, two samples measured in both directions on a test silicon.

In a similar way the rail clamps C1 and C2 were measured and their electrical model was created. In the forward direction the clamps have Von=0.35V and Ron=1ohm. In the reverse direction (Dr_{C1} and Dr_{C2}) the equivalent circuit contains Von=0.6V and Ron=1ohm. The bulk diode of the PMOST was also modeled by Von=1ohm and Ron=1ohm. The resulting simulation model of the circuit is shown in Fig. 5.3.

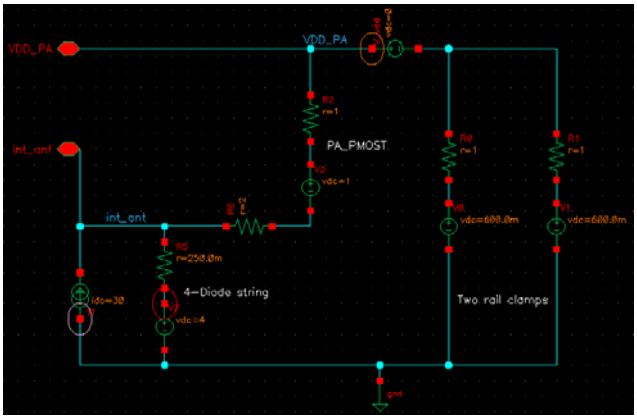

Fig. 5.3. Simulation model of the system for the positive IEC pulse at Int_Ant pin.

The 8kV IEC stress consists of the first short 30A current peak which can generate the overvoltages in the circuit and the second 16A current peak which can damage the components by inducing thermal damage. One simple approach to the simulation is to use a DC current source of a maximum current value (30A and 16A) and check the DC currents that flow through all the circuit elements.

The result of such a simulation is shown in Fig. 5.4. The second 16A current pulse was brought to the circuit. The simulation shows that there are no large overvoltages in the circuit nodes. The maximum node voltage is V(Int_Ant)=7.44V, which is lower than the breakdown voltage (8.2V) of the gate oxide connected to this node.

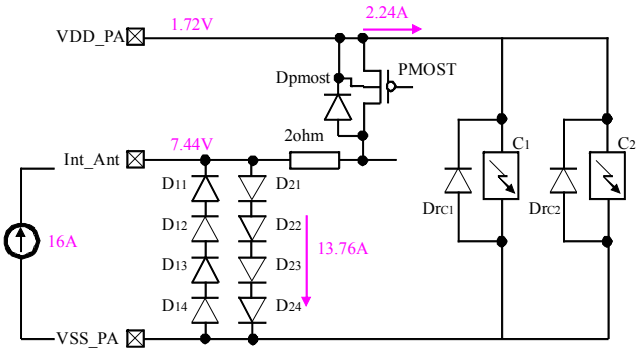

Fig. 5.4. Simulation model of the system for the positive IEC pulse at Int_Ant pin.

The maximum of 13.76A flows through the diode string D21-D41. This is safe since the diodes were designed for 14A. The simulation also shows that 2.24A flows through the unwanted path – through the Dpmost and two clamps C1/C2. Based on the size of the PMOST (720um) it can be

estimated that Dpmost can stand as much as 720um*10mA/um=7.2A. Hence, Dpmost will not be damaged. Two rail clamps C1/C2 are designed to be able to survive as much as 4A of 100ns TLP current (to stand 200V MM stress). Obviously, they will also be able to conduct 2.24A current.

The 2ohm resistor represents the estimated resistance of the relatively long and thin metal connection between the Int_Ant pad and the PMOST. Unfortunately, this connection was not carefully reviewed during the ESD review of the circuit before the production. As a result, the gun test on the produced IC showed circuit failure at 6.5kV stress level instead of targeted 8kV. The failure analysis (FA) of the failing samples showed that the connection towards the PMOST was lost. The weakest point on the metal connection were three 1.9um wide lines in M3 which melted, as visible in Fig. 5.5.

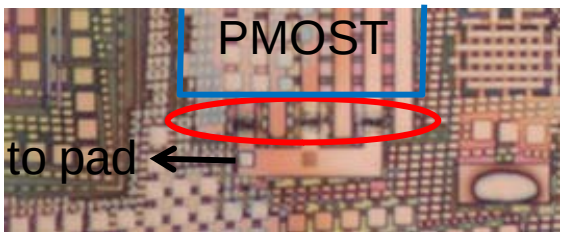

Fig. 5.5. The failure analysis result, three melted M3 lines at PMOST's drain.

A M3 line in the used 45nm process can conduct maximum 225mA of the 100ns TLP current per micrometer of the line width. That means that these three parallel M3 wires could conduct maximum 3*1.9um*225mA/um=1.28A, which confirms the root cause of the fail.

VI. Conclusion

In this paper we defined the pre-requisites for ESD simulation. The modelling of the ESD devices is explained and a case study is given that proves the usefulness of the ESD simulations. In this case, we show that quite simple DC simulation of the circuit is able to explain the root cause of the gun test fail.

One should be careful when simulating ESD since the currents and/or voltages often exeed the valid range of the component models. Therefore it is always recommended to calibrate the simulation results using the measured TLP characteristics of the silicon test structures.

The bigFETs (which are the most popular ESD devices in technologies below 90nm) can be accurately simulated. The simulation of the pad-ring is obligatory when defining the ESD rules in the rail-based ESD concept.

Only the snap-back ESD devices cannot be simulated due to the negative resistance region in their I/V curve. They can be modelled by the Vt1 and Ron, but the designer must be aware that the simulation result becomes invalid as soon as the voltage on the snap-back device exceeds Vt1.

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